Amendments to the Specification

Please replace the paragraph beginning on page 8, line 3, with the following rewritten paragraph.

Turning to the drawings, exemplary embodiments of a method for processing a semiconductor topography are shown in Figs. 1-12. In particular, a method is provided which includes etching one or more layers in an etch chamber while introducing a noble gas heavier than helium into the etch chamber. In a preferred embodiment, the introduction of such a noble gas may reduce the formation of or remove defects within an etched portion of the semiconductor topography. Fig. 1 depicts a partial cross-sectional view of semiconductor topography 20 in which a plurality of layers is formed upon and in contact with each other. In particular, semiconductor topography 20 may include dielectric 24 interposed between semiconductor layer 22 and stack of layers 33. In some cases, dielectric 24 may be regarded as part of stack of layers 33. Alternatively, dielectric 24 may be considered separate from stack of layers 33. In addition, resist layer 32 may be formed above stack of ~~layer~~ layers 33. In some embodiments, semiconductor topography 20 may include additional layers formed upon and in contact with one or more of the layers shown in Fig. 1. Alternatively, semiconductor topography 20 may include fewer layers than shown in Fig. 1. For example, dielectric 24 may be omitted from semiconductor topography 20, in some embodiments.

Please replace the paragraph beginning on page 9, line 10, with the following rewritten paragraph.

Layers 26, 28, and 30 may together form stack of layers 33. More specifically, anti-reflective layer 30 may be formed above cap layer 28, which may be formed above device layer 26 to form stack of ~~layer~~ layers 33. In some embodiments, anti-reflective layer 30 may be formed upon and in contact with cap layer 28. In addition or alternatively, cap layer 28 may be formed upon and in contact with device layer 26. In an alternative embodiment (not shown), stack of layers 33 may include additional layers such as dielectric 24 as discussed above or layers interposed between layers 26, 28, 30, and/or dielectric 24. In either embodiment, device layer 26 may be formed above dielectric 24. More specifically, device layer 26 may be formed upon and in contact with dielectric 24. Alternatively, device layer 26 may be formed upon and in contact with semiconductor layer 22 if dielectric 24 is omitted. In general, device layer 26 may

be used to form a process structure of a subsequently formed device. Such a structure may be a gate conductor or an interconnect line, for example. As such, device layer 26 may include a conductive layer such as, doped polysilicon, aluminum, copper, titanium, tungsten, or a metal alloy. Device layer 26 may have a thickness, for example, between approximately 300 angstroms to approximately 3000 angstroms. However, larger and smaller thicknesses of device layer 26 may be used depending on the specifications of the device.

Please replace the paragraph beginning on page 11, line 16, with the following rewritten paragraph.

After patterning device masks 34, exposed portions of semiconductor topography 20 may be etched as shown in Figs. 3-5. In particular, exposed portions of anti-reflective layer 30 may be etched to form device masks 36 as shown in Fig. 3. Fig. 4 illustrates the removal of exposed portions of cap layer 28 to form structures 38, while Fig. 5 shows the formation of structures 40 subsequent to the removal of exposed portions of device layer 26. Such etch processes may be performed continuously until structures 40 are formed. Alternatively, the etch processes may be conducted in stages. In this manner, cleaning processes may be interposed between the one or more etch processes of stack of layers 33.

Please replace the paragraph beginning on page 14, line 24, with the following rewritten paragraph.

As stated above, conventional etch processes typically produce defects within an ~~etch~~ etched semiconductor topography. Depending on a defect's size, location, and composition, a defect within a device may cause a failure within a subsequently formed integrated circuit. Defects from conventional etching processes may include a variety of shapes and compositions. For example, in an embodiment in which a semiconductor topography comprising a nitride layer and a polysilicon layer is etched, nitride and polysilicon bilayer defects may be formed. In contrast, in an embodiment in which a semiconductor topography comprising an oxide layer and a monocrystalline silicon layer is etched, oxide and monocrystalline silicon bilayer defects may be formed. Such clumps may be cylindrically shaped with a portion of nitride or oxide formed upon a portion of polysilicon or monocyrstalline silicon, respectively. Other defect compositions may be formed during the etch process depending on the compositions of the layers of the topography. In particular, the composition of the defect formed during the etch process may depend on the

materials included in cap layer 28 and device layer 26. A semiconductor topography with a thermally grown silcon nitride layer, however, may be particularly susceptible to such defect formations.

Please replace the paragraph beginning on page 21, line 23, with the following rewritten paragraph.

As ~~state~~ stated above, the introduction of a noble gas heavier than helium into an etch chamber during an etching process may advantageously reduce, prevent, or eliminate the production of defects. As such, the etch processes of Figs. 8, 9, and 11, are preferably conducted such that the formation of defects within etched portions of semiconductor topography 50 is reduced, prevented, and/or eliminated. In particular, the formation of defects comprising bilayer mounds may be reduced, prevented, and/or eliminated during the etch processes of Figs. 8, 9, and 11. More specifically, the number of bilayer defects produced by the etch processes of Figs. 8, 9, and 11 may be reduced to be between 0 defects/cm^2 and approximately 3 defects/cm^2. Such a reduction and/or elimination of defects may advantageously produce a greater number of functional devices within a given lot of wafers.